UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/444,173	11/19/99	PONG	F HP10981470-1

TM02/1010

IP ADMINISTRATION
LEGAL DEPARTMENT 20BN
HEWLETT PACKARD COMPANY
P O BOX 10301
PALO ALTO CA 94303-0890

EXAMINER	
SONG, I	
ART UNIT	**PAPER NUMBER**
2187	5

DATE MAILED: 10/10/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/444,173	PONG, FONG	
	Examiner	Art Unit	
	Jasmine Song	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. For example:

Page 7, lines 10, "Each of the processors and memory main memory" should be changed to "Each of the processors and main memory".

Claim Rejections - 35 USC § 102

2. The rejection of claims 1-20 is **maintained**.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al., U.S. Patent 6119204.

Regarding claims 1,9 and 19, Chang et al. teach a method for accessing memory in a multiprocessor system, the method comprising:

from a requesting processor, issuing a request for a block of data to one or more

other processors and memory is taught as interconnect 16 includes a broadcast fabric , each device connected to interconnect 16 preferably snoops all communication transactions on interconnect 16 (Fig.1, 2 and 3, col. 7, lines 35-38 and col.4, lines 23-34), each copy of the block of data being associated with state information indicating whether the copy is valid or invalid is taught as sourcing data cached within cache hierarchy 36 on interconnect 16, updating the coherency state of cached data, invalidating entries within the TLB of processor 10 (Fig.2, col.4, lines 47-62);

in each of the processors and memory that receive the request, checking to determine whether a valid copy of the block of data exists (col.7, lines 39-43); and

returning a valid copy of the requested data from one of the other processors or memory such that only the processor or memory having the valid copy of the data block responds to the request (col.11, lines 44-54).

Regarding claims 2 and 10, Chang teach each of the processors communicates with the memory via a memory controller (col.4, lines 20-22) and each of the processors has a point-to-point link with the memory controller for issuing a request for a block of data to the memory controller (Fig.1 & Fig.2).

Regarding claims 3 and 11, Chang teach each point-to-point link includes two dedicated and unidirectional links (Fig.2, the lines indicating " to interconnect" and "from interconnect").

Regarding claims 4 and 12, Chang teach the point-to-point links are control links for sending and receiving requests for blocks of data (Fig. 2)

Regarding claims 5 and 13, Chang teach each of the processors has a control path point-to-point link for sending and receiving requests for blocks of data, and a data path point-to-point link for sending and receiving blocks of data (Fig. 2).

Regarding claim 6, Chang teach the processors and shared memory that have an invalid copy of the requested block of data drop the request without responding (col.11, lines 44-54)

Regarding claim 7, Chang teach tracking an identification of a processor that currently has a data block (Fig. 3, element 92); and in response to a cache miss in a requesting processor (Fig. 3), using the identification to specifically target a read request to the processor that currently has the requested data block (Fig. 3, col.7, lines 12-38).

Regarding claim 8, Chang teach maintaining a directory indicating the one or more processors that have a copy of a block of data (Fig.3 element 84); when the block of data is modified, using the directory to issue a write invalidation or write update only to the processors that have the copy of the block of data (col.7, lines 6-12).

Regarding claims 14,15 and 16, Chang teach a directory indicating which processors have a copy of a data block; wherein the processors are in communication with the directory to identify which other processors have a copy of the data block, and directing requests for the data block only to processors that have a copy of the data block (Fig. 3, col.6, lines 53 to col.7, lines 38).

Regarding claim 17, Chang teach the memory controller is in communication with a shared cache, separate from caches of the processors, for buffering most frequently accessed data block (col.7, lines 2-5).

Regarding claims 18, Chang teach each block has state information indicating which processor currently has a valid copy of a data block, and wherein the processors utilize the state information to specially address a processor having the valid copy in response to a cache miss in a requesting processor (Fig. 3, col.6, lines 47 to col.7, lines 2).

Regarding claim 20, Chang teach each of the processors and the shared memory is in communication with a control path interconnect, and each of the processors is in communication with the control path interconnect via a point-to point link for receiving and sending requests for blocks of data (Fig. 1 and Fig.2);

each of the processors having a corresponding request queue connecting the

point-to-point link of the processor to the control path interconnect (col.8, lines 34-40), and each of the processors having a corresponding snoop queue connecting the point-to-point link of the processor to the control path interconnect (col.4, lines 53-62);

the request queue in communication with a corresponding processor for buffering requests for blocks of data by the processor and issuing the requests to other processors via the control path interconnect (col.4, lines 49-53); and

the snoop queue in communication with a corresponding processor for buffering requests for blocks of data destined for the processor (col.4, lines 53-63).

Response to applicant's Arguments

5. In response to applicant's argument that Chang's reference does not teach coherency between memory systems. It is noted that Chang's reference teach maintaining TLB coherency, his reference also teach coherency between memory systems (col.7, lines 39-43).

6. In response to applicant's argument that Chang's reference does not have the limitation of "a request for a block of data to one or more other processors and memory". It is noted that this limitation is implied in Chang's reference because one of the processors have to send the request for a block of data in order to know which processor has the ownership to access the memory system. Also, It is noted that Chang's reference teach data requests or memory mapped I/O issued on interconnect by BIU which means send data request to one of processor and memory system (Fig.1 and 2 and 3, col. 7, lines 35-38).

Conclusion

7. Applicant's arguments filed 08/06/2001 have been fully considered but they are not persuasive.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do H Yoo can be reached on 703-308-4908. The fax phone numbers for

the organization where this application or proceeding is assigned are 703-305-9731 for regular communications and 703-305-9731 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

October 9, 2001

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100